

양자 컴퓨팅을 위한 극저온 저잡음 증폭기 MMIC 개발



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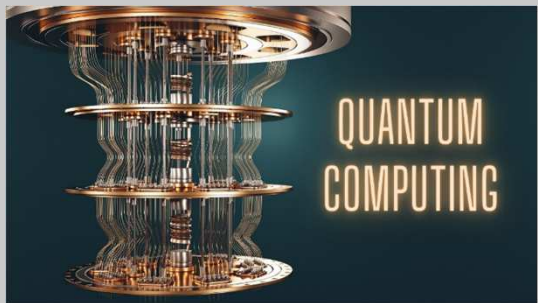
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양자컴퓨팅(Quantum Computing)



What is Quantum Computing ?

양자 컴퓨팅(Quantum Computing)



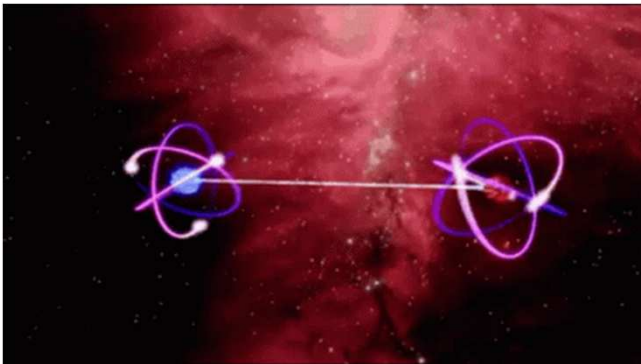
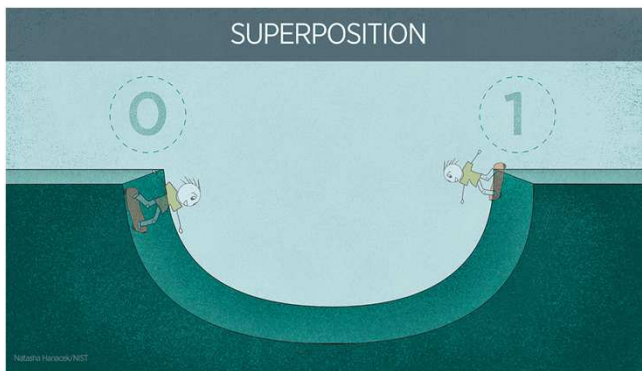
Quantum Computing Market Forecast



- CAGR 35.3% (2021 – 2031)
- Market Value : USD 14Billions(약 18조원) - 2031
- Hardware 시장
 - 1) 전체 시장의 25% 점유
 - 2) Market Value : USD 3.25Billions(약 4.5조원) -2031

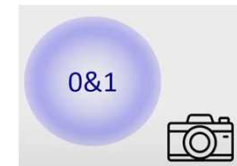
What is Quantum Computing ?

양자역학을 활용한 양자 컴퓨팅의 원리

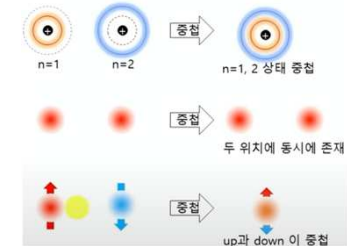


● 양자중첩 (Superposition)

✓ 양자 역학 : 0이면서 1인 상태

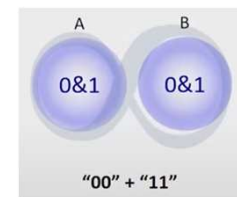


관측하는 순간
두 상태중 하나로 붕괴



● 양자얽힘 (Entanglement)

✓ 양자 역학 : 여러 개의 입자의 양자 상태가 서로 얽혀있는 (= 따로 떨어뜨려서 생각할 수 없는) 상태가 존재



What is Quantum Computing ?

양자 컴퓨팅(Quantum Computing)



컴퓨터를 만들기 위한 조건

조건	기존 컴퓨터	양자 컴퓨터
무엇을 이용할 것인가?	전기(전류가 흐르는 상태를 1, 그리고 전류가 흐르지 않는 상태를 0)	양자역학적 중첩상태(1과0은 동시에 존재)
제어할 수 있는 하드웨어가 있는가?	트랜지스터	양자역학적 특성을 보이는 모든 것 사용 가능(원자, 빛, 스핀, 초전도체)
하드웨어를 이용해서 Gate Operation을 할 수 있는가? Universal gate가 있나?	AND, OR, XOR, --- NAND는 Universal gate	NOT, CNOT gate
Gate들을 잘 연결해서 계산이 가능한 알고리즘이 있는가?	AND+XOR의 조합으로 덧셈을 하는 등의 알고리즘	개발중(몇가지 보유)
그래서 무슨 문제를 푸는가?	사칙연산을 이용한 다양한 응용	암호 해독, 최적화된 경로, 자연을 시뮬레이션

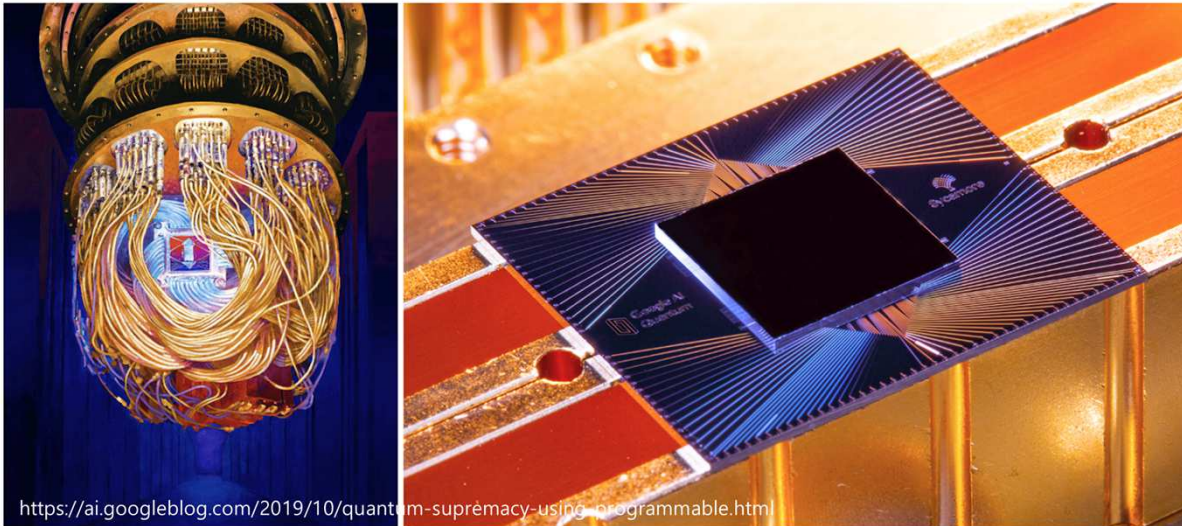
- 초전도 큐비트(superconducting loops)
- 원자이온(Trapped ions)
- 중성원자(Neutral Atoms)
- 광자(Photonics)

Quantum Computing Type

양자 컴퓨팅(Quantum Computing)



초전도 큐비트(superconducting loops)



현재 가장 성숙한 플랫폼1

마이크로파로 양자비트를 제어

최근 IBM 433 큐비트 발표

대표 기업 : 대기업 주도

Google, IBMQ, Microsoft,...

장점

- ✓ 양자비트를 칩으로 만들수 있다
- ✓ 뛰어난 제어능력

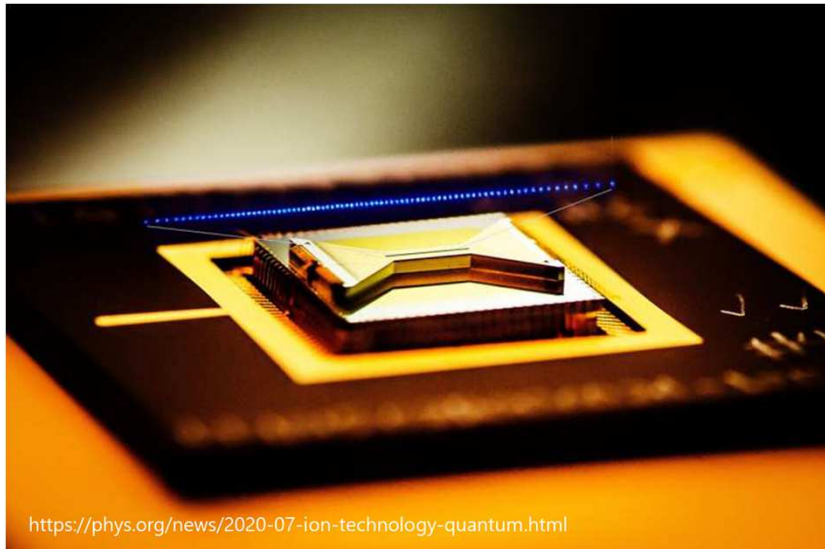
단점

- ✓ 극저온 장치가 필요(수mK)
- ✓ 확장성에 취약



1,000 큐비트가 한계
따라서 병렬방식으로 네트
워킹하여 진화 필요

원자이온(Trapped ions)



장점

- ✓ 모든 양자비트가 동일(결함 X)
- ✓ 뛰어난 제어능력

단점

- ✓ 개별 양자 비트의 제어에 취약
- ✓ 확장성에 취약

현재 가장 성숙한 플랫폼2

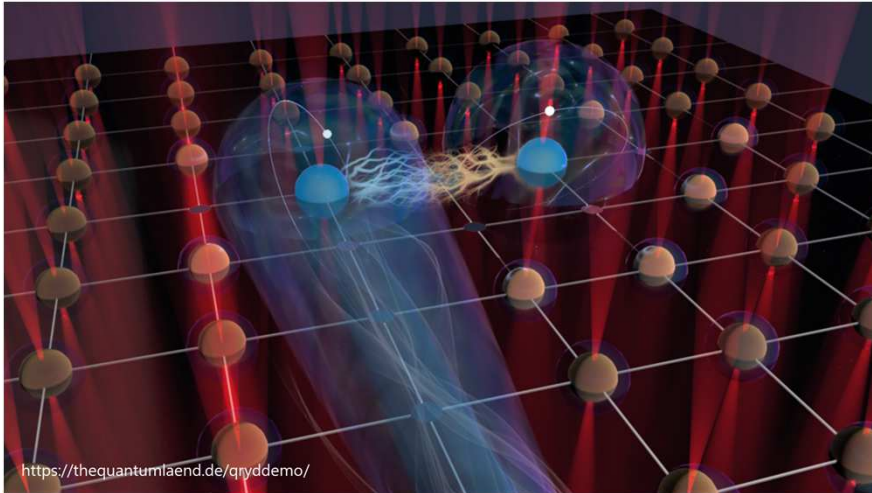
레이저로 양자비트를 제어

- 1) 원자이온의 레이저냉각
- 2) 진공상태에서 원자하나를 띄워놓고 전기장으로 담아 사용

현재 약 50~100여개의 양자비트

대표 기업 : Honeywell(now Quantinuum),
ION_Q, ...

중성원자(Neutral Atoms)



장점

- ✓ 모든 양자비트가 동일(결함 X)
- ✓ 뛰어난 확장성 & 제어가능성

단점

- ✓ 시스템 장치 사이즈가 크다 (진공장치, 레이저 등등)
- ✓ 개별 양자 비트의 제어에 취약

Catching up 플랫폼1

레이저, 마이크로파로 양자비트를 제어

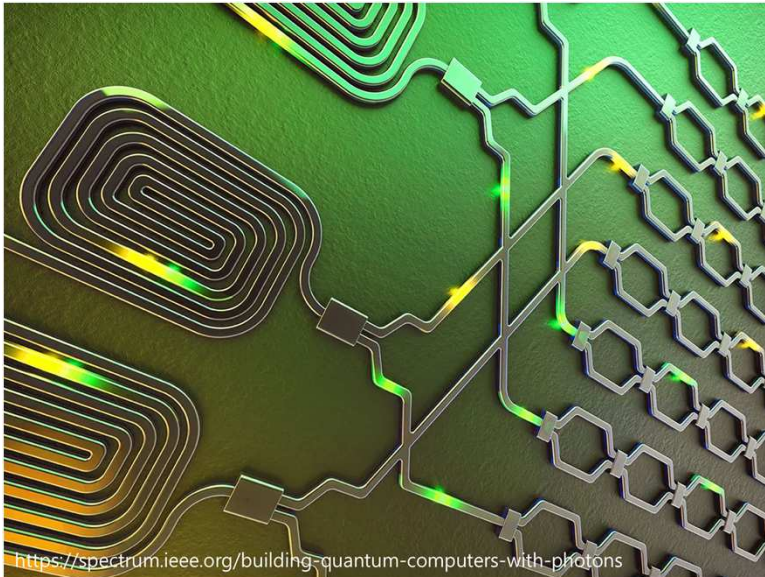
- 1) 루비듐, 리튬같은 원자를 이용
- 2) 레이저를 포커스(레이저가 인텐시티가 높은 강한곳에 원자가 끌리는 성질 이용)하여 광집계를 만들어 집계로 만들어 원자를 가두어 사용

현재 수백개의 양자비트

대표 기업 : Quera, Cold Quanta, PASQAL,

...

광자(Photonics)



장점

- ✓ 상온에서 동작
- ✓ 양자 통신과의 수월한 연결 가능성

단점

- ✓ 취약한 제어능력(큰 연산 오류 가능성)
- ✓ 제한적인 양자 연산

Catching up 플랫폼2

측정기반의 양자컴퓨터

- 1) 광이 설계된 길을 따라서 빛이 진행되면서 알아서 연산이 되어서 나오는 결과물을 보고 해석하는 장치
- 2) 광자가 광파로를 통해 두갈래길을 교차시키고 광이 가는 방향을 중첩과 얽힘을 만드는 방식

현재 약 100여개의 양자비트

대표 기업 : Xanadu, PsiQuantum, ORCA,

...

Quantum Computing Application

양자 컴퓨팅(Quantum Computing)



Big Data



<https://www.koreaherald.com/view.php?ud=20210901001000>

Security



<https://www.science.org/content/article/worried-quantum-computers-will-supercharge-hacking-white-house-calls-encryption-shift>

Optimization problems

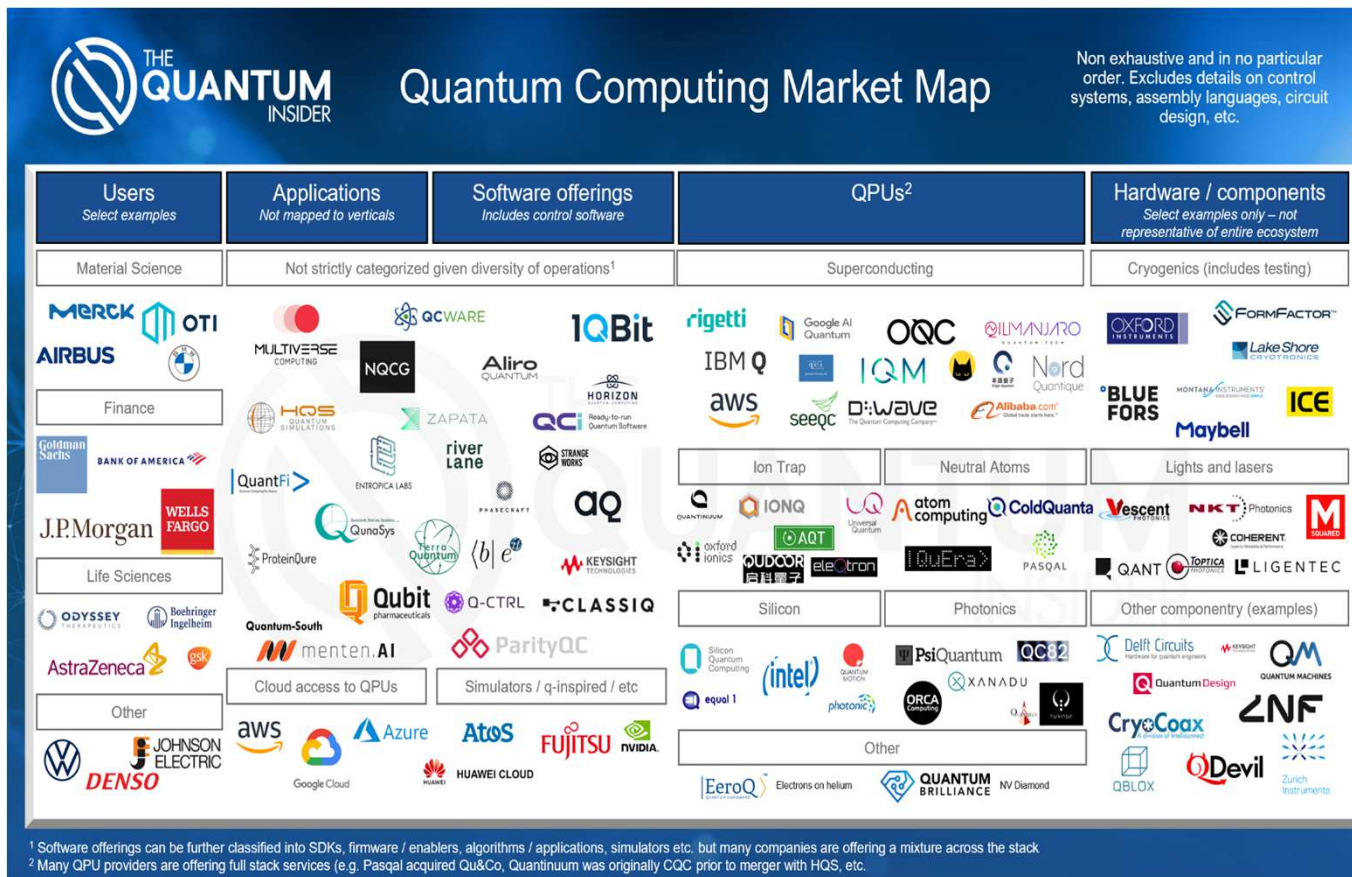


<https://www.pathstone.com/quantum-computing-for-a-chemical-world/>

분야	응용 예	사례
금융	- 포트폴리오 최적화 - 리스크 관리 - 옵션 가격 결정	- 2016년, D-Wave system와 1QBit가 "Quantum for Guants" 설립
물류	- 비행기, 선박, 트럭 등의 물류 최적화	- PLC와 Manchester Met. 대학의 물류 알고리즘 공동 개발
화학	- 분자 설계 최적화 - 화학 반응의 양자 역학적 시뮬레이션 - 전자와 촉매의 최적화	- IonQ의 화학 시뮬레이션 SW개발 - MS의 기초 연구 - ETH, Harvard대학 등의 연구 등
제약	- 단백질의 3차원 구조 최적화/분석(알츠하이머병 등 특효약 개발)	- Stanford 대학의 "Folding@home" 프로젝트 - Harvard 대학/D-Wave Systems의 단백질 분석 실험
의료	- 암치료용 약물 발견/ 최적복용량 산출 - 개인 맞춤형 의료의 고속화	- Stanford대학, Texas대학에서 연구
자동차	- 도시 교통 서비스 최적화	- Volkswagen과 Google의 공동개발 및 Volkswagen의 주문형 이동 서비스를 위한 알고리즘 개발
IT	- 머신 러닝을 위한 고속 클러스터링 - 이미지 인식 고속 학습	- Google/D-Wave Systems의 이미지 인식 정확도 향상 - (중) USTC, NMR 기술 이용 4큐비트 양자 프로세서 개발
항공우주	- 유체 역학적으로 최적화된 기체 설계 - 비행 제어 시스템의 버그잡기 최적화	- NASA의 비행체 날개 설계 최적화 - Lockheed Martin과 Airbus의 제어 시스템 버그 탐색 SW개발 (6개월 - > 6주)

양자 컴퓨터의 생태계 및 당면 과제

양자 컴퓨팅(Quantum Computing)



다양한 기반 기술 필요

- Microwave tech.
- Laser tech
- Optical tech.
- Vacuum tech.
- Low temperature tech.
- Classical Computations

현재 각 플랫폼의 양자비트 개수 (클라우드 서비스 기준)

- 초전도큐비트 : 433개 IBM Q
- 이온 : 23개  IONQ
- 중성원자 : 256개 
- 광자 : 216개 

필요한 양자비트의 개수

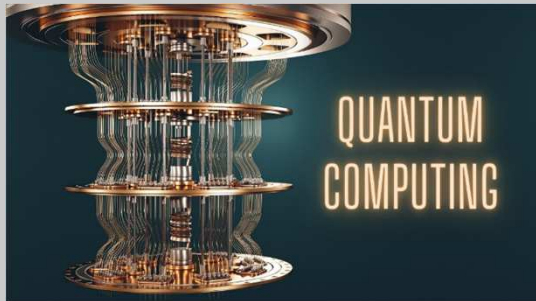


양자컴퓨터 활용분야

Source: "Nature." Wikipedia ©2019 Gartner, Inc. All rights reserved.

당면 과제

제어의 정확도를 유지하며 양자비트의 개수 늘리기
새로운 플랫폼의 탐색



Cryogenic LNAs (Low Noise Amplifier) 개발

Cryogenic Electronics – Cryogenic LNAs

Google: Martinis, Nature (2019) → 54 qubit system (presently w/ UCSB)

Currently, Cryogenic LNAs (CLNAs) have been widely used to readout a noisy qubit signal!

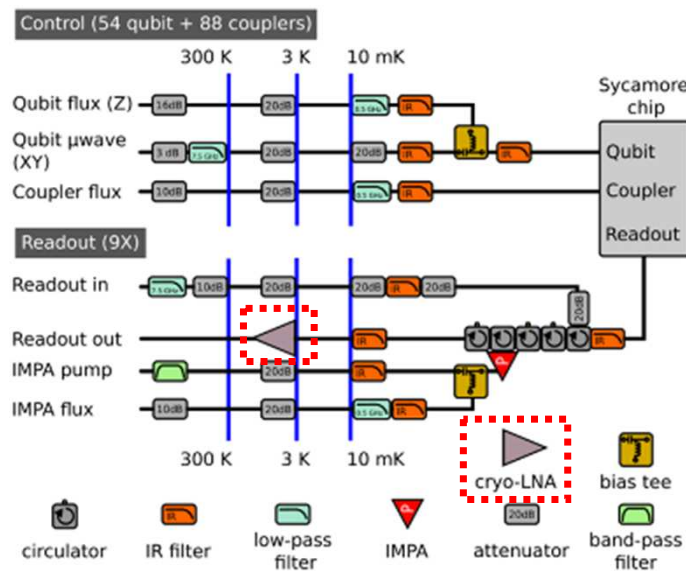
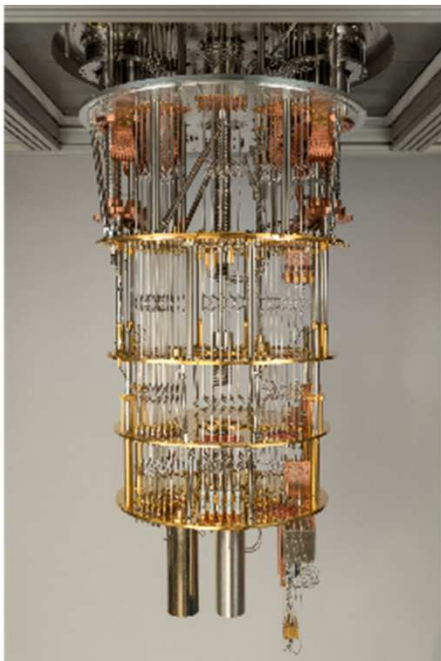
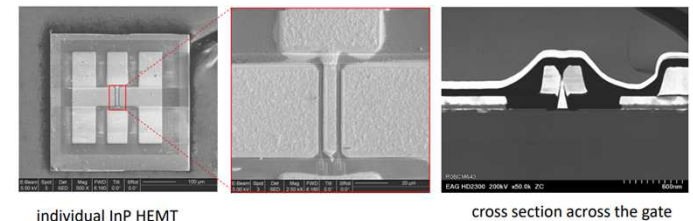
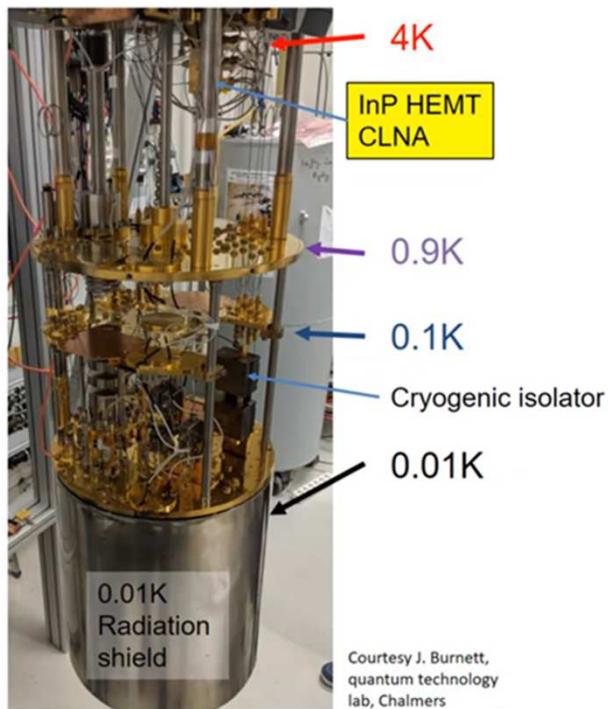


Figure S3: Cryogenic wiring. Control and readout signals are carried to and from the Sycamore chip with a set of cables, filters, attenuators, and amplifiers.

- Readout of microwave photons -130 dBm at 4-12 GHz
- For 30 years, PHEMTs have been the choice for CLNAs, first GaAs, and then $\text{In}_x\text{Ga}_{1-x}\text{As}$, $x > 0.53$
- InP HEMT hybrid 4-8 GHz CLNAs typically used as 2nd stage amp (4K stage)

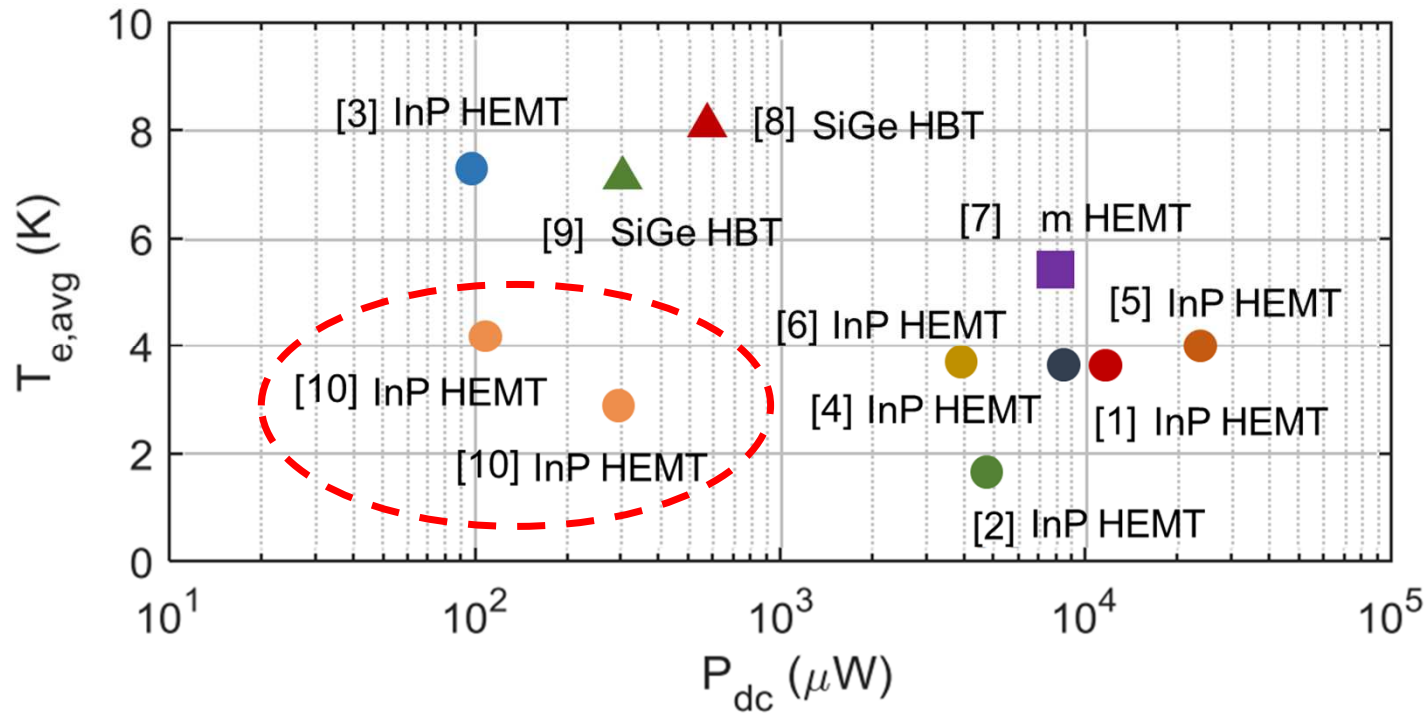


InP HEMT's Advantages as Cryogenic LNAs



- Circuit
Superconducting parametric amplifier at the mK stage
→ CLNAs at the 4 K stage is used for readout as the 2nd amplifier
- Cryogenic LNAs : One of the key components in the readout chain
- Request
 - 1) Lower noise figure at C-band
 - 2) Lower power dissipation(DC)
- Today use normally based on InP high-electron-mobility transistors (HEMTs) only
- Why InP HEMT as cryogenic LNAs
 - 1) the lowest noise figure at C-band in comparison with any other transistor technology
 - 2) the HEMT can be scaled down to improve the ratio of transconductance to drain current at low drain voltage

InP HEMT's Advantages as Cryogenic LNAs



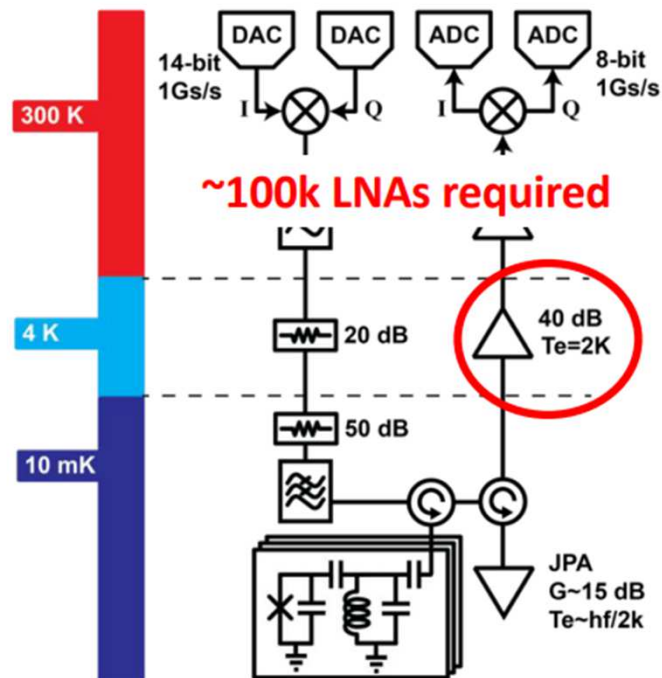
Comparison of the average noise temperature of LNAs with prior state-of-the-art results operating in C-band at cryogenic temperature.

InP HEMT's Advantages as Cryogenic LNAs

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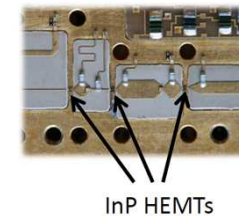
Future Readout of 1M Qubit Processor



출처 : SiGe Cryogenic Amplifiers for Superconducting Qubit Readout Joseph C. Bardin(1,2), (1)University of Massachusetts Amherst, (2)Google Quantum AI @IEEE. IMS 2023

Today :

- InP LNA only
- Hand assembled, individually tested



Future :

Improvement of InP HEMT LNAs

- Robust and low cost μW cryogenic LNAs manufacturing
- Scaling LNAs module \rightarrow Integrated circuit(MMIC LNA)
- Lower power dissipation

양산을 위한 Cryogenic LNAs MMIC 개발

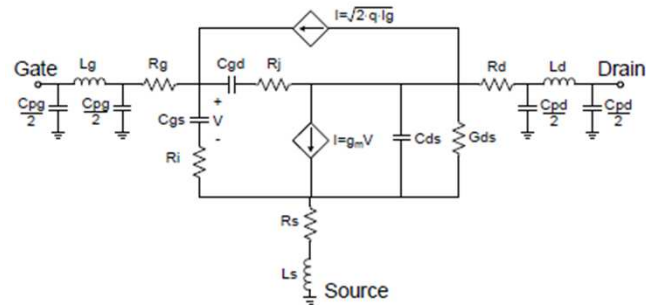
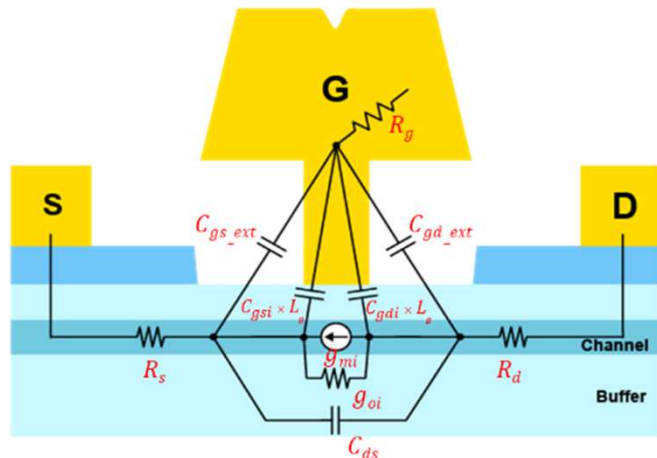


InP HEMT – Noise Model

Cryogenic LNAs(Low Noise Amplifier) 개발



Noise sources in cryogenic HEMT LNAs



$$\text{Minimum noise temp: } T_{\min} \approx 2 \frac{f}{f_T} \sqrt{(R_s + R_g + R_i) T_g G_{ds} T_d}$$

300K breakdown @ 6GHz

Parameter	Contribution in Kelvin	Contribution in %
Input matching network	7.1 K	24%
Rg	2.6 K	9%
Ri	6.3 K	21%
Rs	2.5 K	8%
Rgd	2.7 K	9%
Channel (Rds)	7.1 K	24%
Rd	0.3 K	0%
Subsequent stages	1.3 K	4%
Sum	29.9 K	≈100%

Input=71%

4K breakdown @ 6GHz

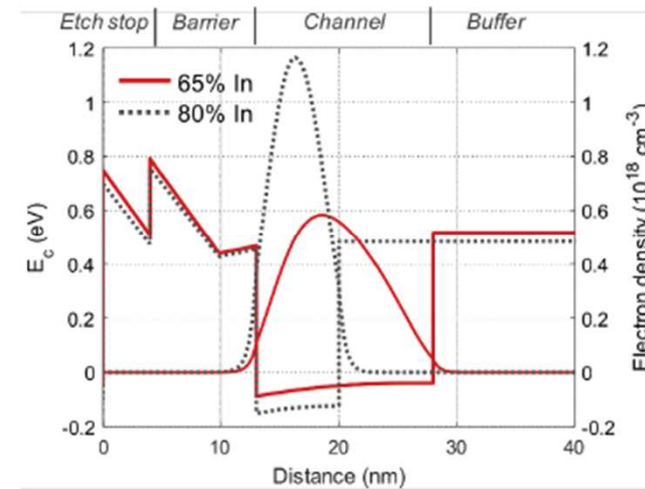
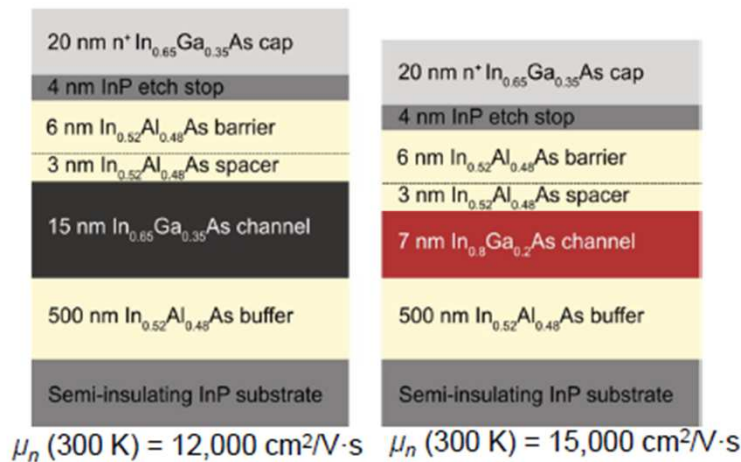
Parameter	Contribution in Kelvin	Contribution in %
Input matching network	0.05 K	3.5 %
Rg (@ 10K)	0.03 K	2.1 %
Ri	0.06 K	4.2 %
Rs	0.03 K	2.1 %
Rgd	0.04 K	2.8 %
Channel (Rds)	1.12 K	79.4 %
Rd	0.00 K	0.0 %
Subsequent stages	0.08 K	5.6 %
Sum	1.41 K	≈100%

Input=15%

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing",
1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahm, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of In channel composition : simulation @ RT

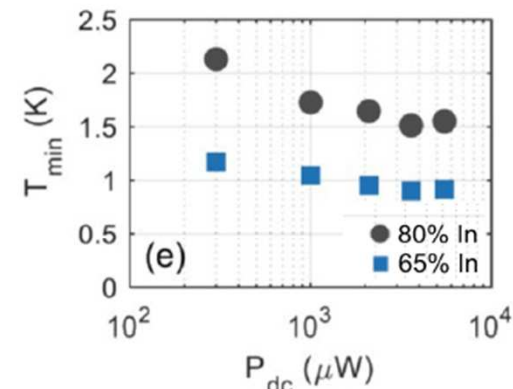
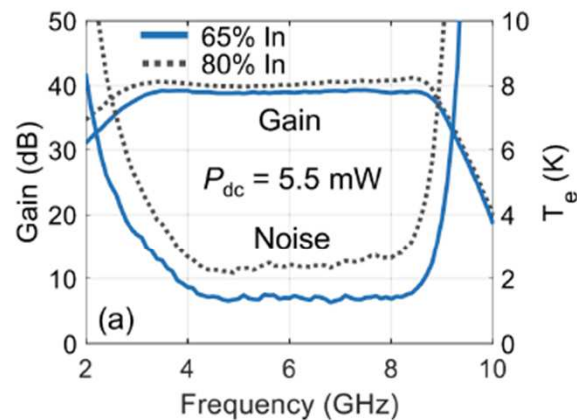
- InP HEMTs with different indium channel content, 65% and 80%, were studied
- The 2DEG in the 80% indium channel HEMT was much closer to the gate leading more efficient charge control



출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of In channel composition : in 4-8GHz CLNA

- The 65% indium channel HEMT: $T_{e,avg} = 1.4$ K, gain = 39 dB
- The 80% indium channel HEMT: $T_{e,avg} = 2.4$ K, gain = 40 dB

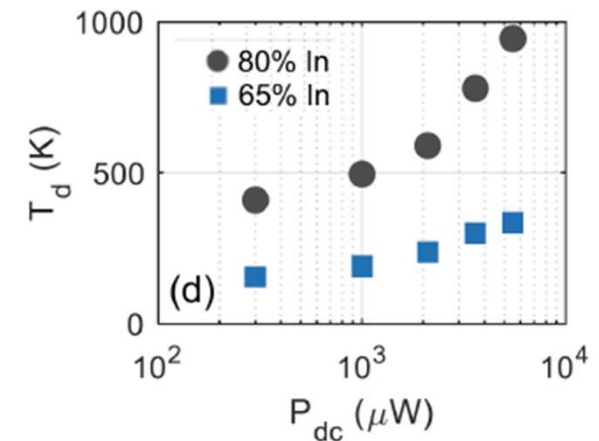


Cha et al. IEEE Trans. Electron Devices 2023

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahm, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of In channel composition

- Noise performance at 300 K was comparable for both
- 65% In channel HEMT LNA exhibited significantly lower noise at all dc power levels
- Extracted T_d (equivalent drain temp) is higher for 80% In
- Could be due to more electron scattering in the 80% In channel: differences in strain in the channel

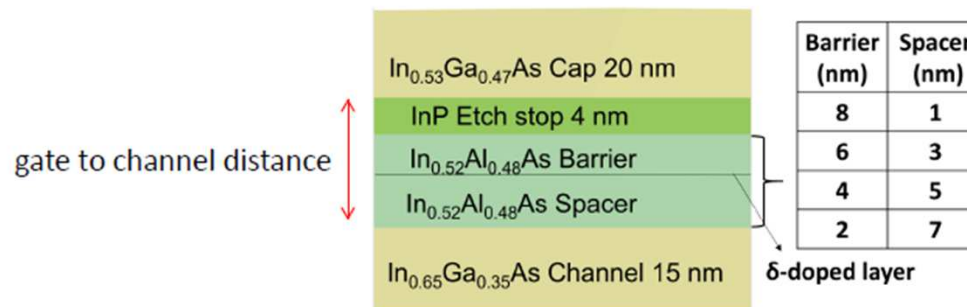


Cha et al. IEEE Trans. Electron Devices 2023

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of spacer thickness

- InP HEMTs with different spacer thickness : 1 to 7 nm
- Barrier thickness has adjusted accordingly to maintain the same gate to channel distance (9 nm)

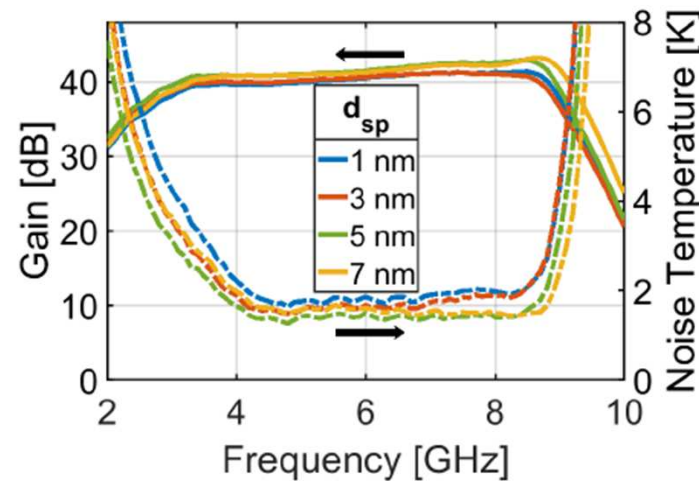


Li et al. IEEE Electron Device Letters 2022

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of spacer thickness : in 4-8 GHz CLNA

- Gain and noise of the HEMTs with different barrier thickness were measured in 4-8 GHz CLNA
- Measured noise was minimum for spacer thickness of 5 nm

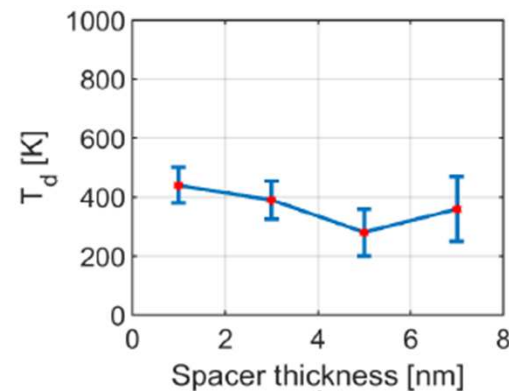


Li et al. IEEE Electron Device Letters 2022

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of spacer thickness : in 4-8 GHz CLNA

- Drain Noise temperature , T_d , was extracted by comparing the measured gain and noise of the LNA with simulations based on an equivalent small-signal HEMT model.
- T_d is minimum for InP HEMT with 5 nm spacer thickness



Li et al. IEEE Electron Device Letters 2022

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

Impact of spacer thickness : real-space transfer (RST)

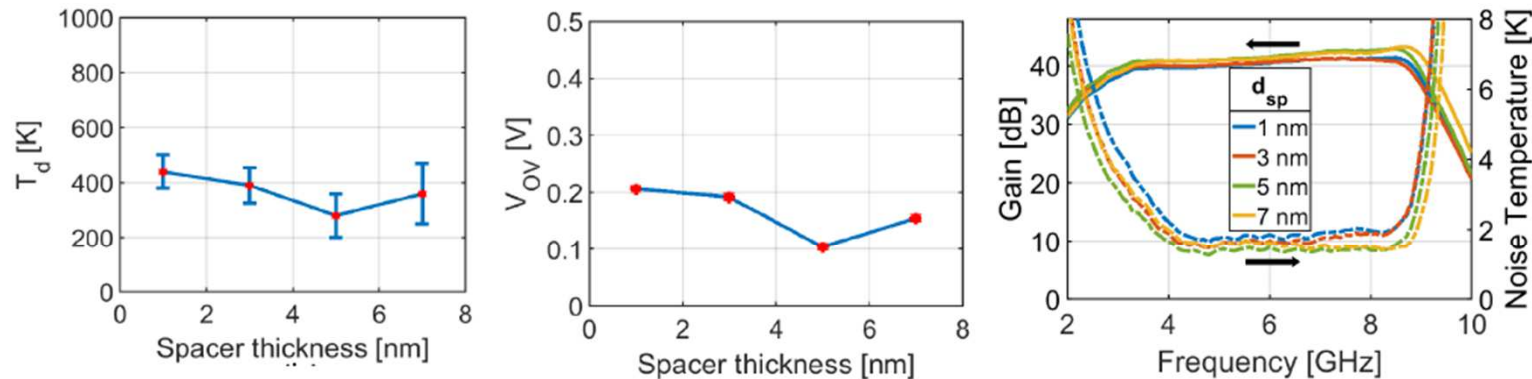
- RST is the emission of 2DEG hot carriers from the channel into the barrier: important source for microwave drain noise
- The overdrive voltage $V_{OV} = V_{gs} - V_{th}$: controls the fraction of transferred electrons
- If RST is responsible for noise in the HEMTs, the noise must be minimized for the lowest V_{OV} at the optimum noise bias

I. Eshoet al. Journal of Applied Physics, 2022

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahn, 1Low Noise Factory, 2 Chalmers University of Technology

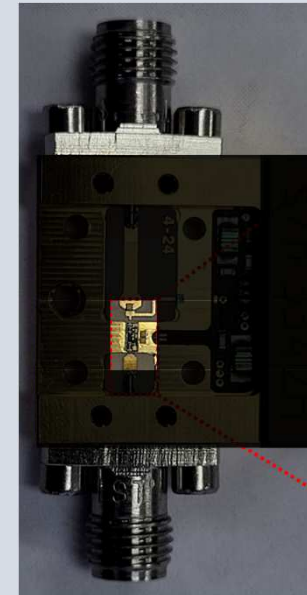
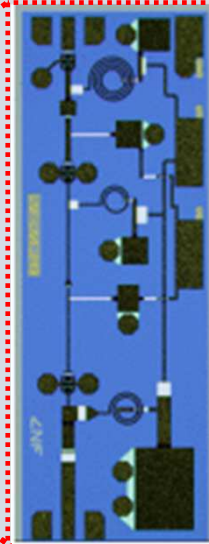
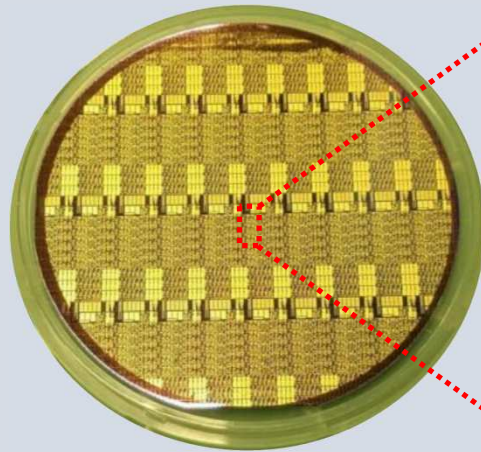
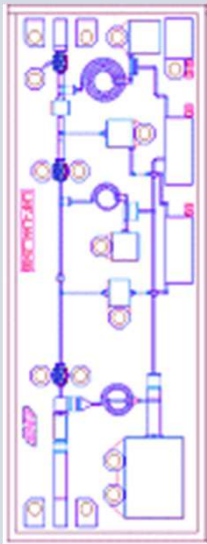
Impact of spacer thickness : in 4-8 GHz CLNA

- The correlation between T_d and V_{OV} at 5 nm spacer thickness suggests that RST noise can be important in cryogenic InP HEMTs



Li et al. IEEE Electron Device Letters 2022

출처 : IEEE, IMS2023, WSF-04, "State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing", 1Arsalan Pourkabirian, 1Johan Bergsten, 1Jörgen Stenarson, 1Niklas Wadefalk, 2Yin Zeng, 2Junjie Li, 2Eunjung Cha and 2Jan Grahm, 1Low Noise Factory, 2 Chalmers University of Technology



2NF

IC 설계



IC 제작

2NF

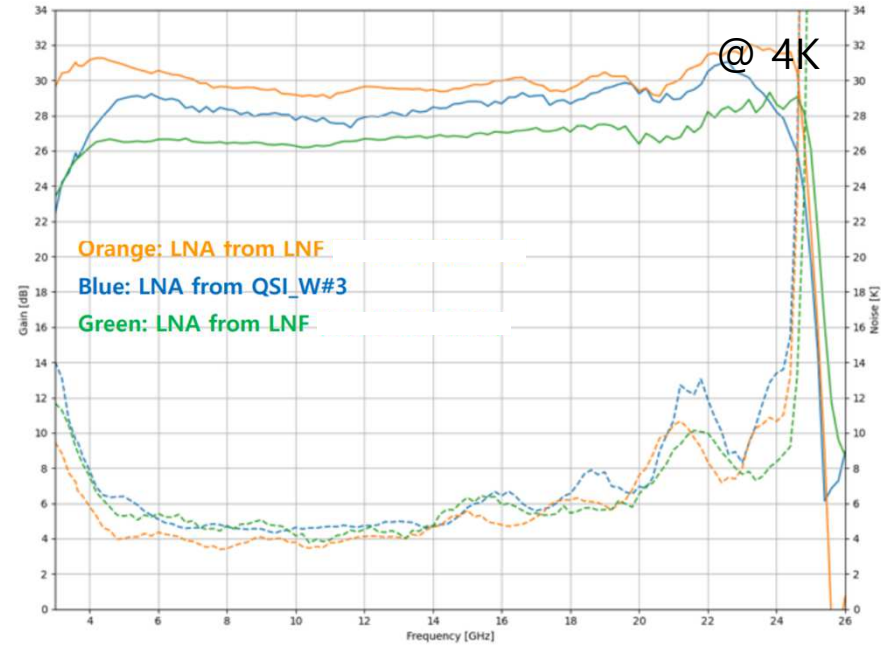
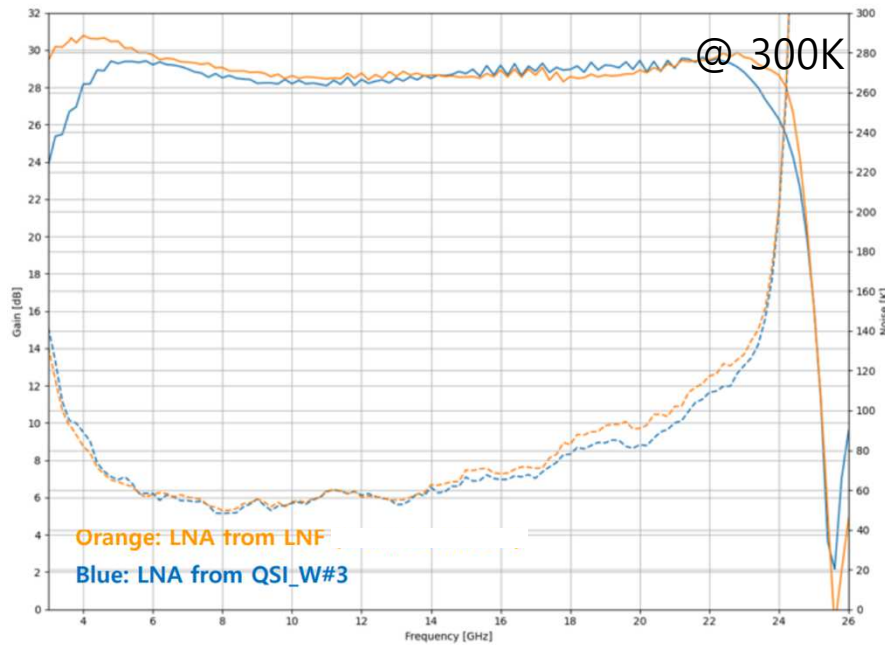
모듈 제작 및 평가

Cryogenic LNA MMIC 개발

Cryogenic LNAs(Low Noise Amplifier) 개발

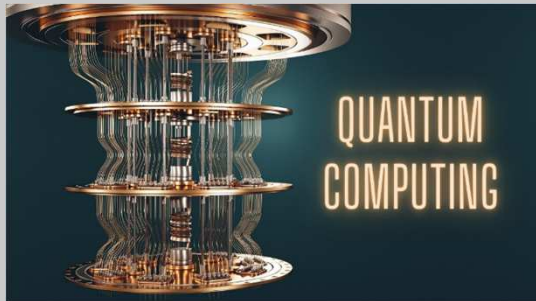


- Gain : 29dB @ 6GHz, 4K
 - Noise Temperature : 5K @ 6GHz, 4K
- LNF사의 상용 LNA와 동일한 성능을 확보함.





파운드리 사업 계획



화합물 광반도체 제조 회사



Epitaxy

- MOCVD
- High Quality Crystal Growth



FAB

- Semiconductor Process Technology
- Optical Coating Technology



Package

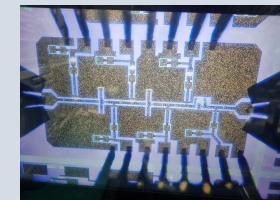
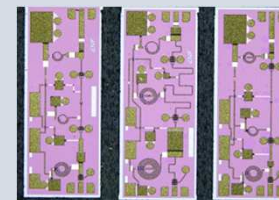
- TO & LeadFrame
- Device Evaluation Technology

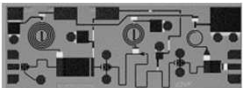
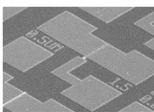
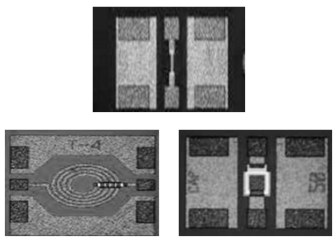
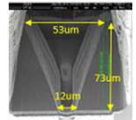
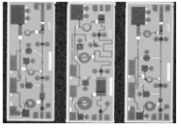
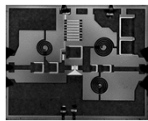
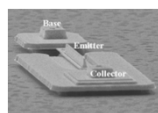


화합물 반도체 전문기업

GaAs, InP기반의 화합물 반도체 파운드리 사업 전개중

InP기반의 HEMT, HBT 소자 중심의 RF Foundry 사업



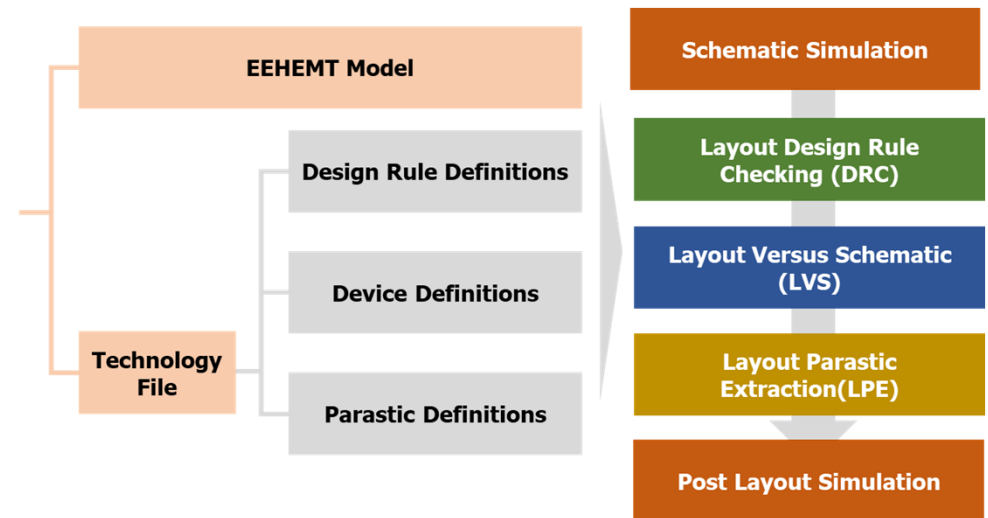
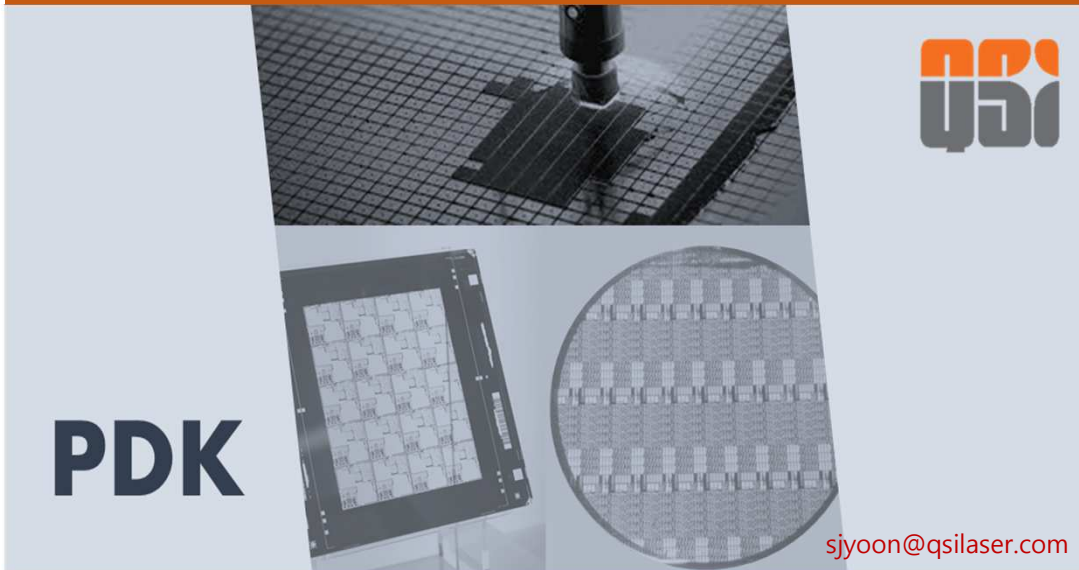
MMIC	FRONT END		BACK END	
	ACTIVE	PASSIVE	VIA	DICING
 <p>LNA</p> <ul style="list-style-type: none"> 과제를 통한 LNA 제작 <ol style="list-style-type: none"> ① L社 Cryogenic LNA ② Sub 6GHz LNA ③ C/X/Ku/K/W-Band LNA ④ W社 LNA 	 <p>HEMT</p> <ul style="list-style-type: none"> 80~500nm HEMT 특성 확보 양산성 확보 	 <p>TFR Capacitor Inductor</p> <ul style="list-style-type: none"> Passive 개발완료 <ol style="list-style-type: none"> ① NiCr TFR ② MIM Capacitor ③ Spiral Inductor 양산성 확보 진행 중 	 <p>T65-D60 T65-D50 T60-D40</p> <ul style="list-style-type: none"> T65-D60 적용 가능 T65-D50 및 T60-D40 개발 중 	 <p>InP Substrate Dicing</p> <ul style="list-style-type: none"> HEMT Discrete Dicing 가능 LNA Chip Dicing 가능
 <p>PA</p> <ul style="list-style-type: none"> TBD 	 <p>HBT</p> <ul style="list-style-type: none"> 2nd Gen. 단위 공정 개발 완료 2nd Gen. 소자 재현성 확보 중 			

• HEMT : High Electron Mobility Transistor
• HBT : Hetero-junction Bipolar Transistor

• TFR : Thin Film Resistor
• MMIC : Monolithic Microwave Integrated Circuit

- 2023년 11월 Process Design Kit 제작 완료 예정
- 2023 ~2024년 PDK 검증 계획
- 100nm Gate Length InP D-mode HEMT기반 서비스
- FAB ~ Dicing 서비스 제공
- 2024년 Epitaxy 공정 내재화 예정
- 2024년 4인치 공정 프로세스 적용 예정

→ 연구기관에 무상 MPW 파운드리 서비스 제공(2024년 초)





Thank you